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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/617,441	07/14/2000	HIROTAKA KAWATA	106310	5358

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EXAMINER	
BROCK II, PAUL E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/617,441	Applicant(s) KAWATA, HIROTAKA	
	Examiner Paul E Brock II	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 20-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *20 August 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: There is no support in the specification for the claim terminology "a semiconductor having a channel region and at least one portion extending outside of the channel region in a gate-width direction perpendicular to a gate length direction that is a direction in which one of the plurality of data lines extends" and "the at least one portion and at least one of a source region and a drain region being separated by an extension of the gate electrode and the extension extending in the gate length direction outside of the semiconductor region."

Drawings

2. The corrected or substitute drawings were received on August 20, 2002. These drawings are approved.

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the at least one portion and at least one of a source region and a drain region being separated by an extension of the gate electrode must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1 – 8 and 20 – 23 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It is not clear where there is support for "the at least one portion and at least one of a source region and a drain region being separated by an extension of the gate electrode" in the originally filed specification.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 3 – 7 and 21 – 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakazawa et al. (USPAT 5614730, Nakazawa).

With regard to claims 1, 21 and 22 Nakazawa discloses in figures 19a – 19c and 20 an electro-optical device or a thin film transistor array substrate. Nakazawa discloses in figures 19a

– 19c and 20 a substrate (109). Nakazawa discloses in figures 19a – 19c and 20 a plurality of scanning lines (101). Nakazawa discloses in figures 19a – 19c and 20 a plurality of data lines (108) on of the data lines crossing one of the plurality of scanning lines. Nakazawa discloses in figures 19a – 19c and 20 a plurality of transistors disposed correspondingly to intersections between the plurality of data lines and the plurality of scanning lines. Nakazawa discloses in figures 19a – 19c and 20 a gate electrode (103). Nakazawa discloses in figures 19a – 19c and 20 a semiconductor (102) having a channel region and at least one portion extending outside of the channel region in a gate-width direction perpendicular to a gate length direction that is a direction in which one of the plurality of data lines extends. Nakazawa discloses in figures 19a – 19c and 20 the at least one portion and at least one of a source region and a drain region being separated by an extension of the gate electrode and the extension extending in the gate length direction outside of the semiconductor region.

With regard to claim 3, Nakazawa discloses in column 4, lines 3 – 12 the semiconductor region forming the transistor comprises polycrystalline silicon.

With regard to claim 4, Nakazawa discloses in column 3, line 57 the substrate being an insulative substance.

With regard to claim 5, Nakazawa discloses in column 3, line 57 the substrate being an quartz substrate.

With regard to claim 6, Nakazawa discloses in column 3, line 57 the substrate being an glass substrate.

With regard to claim 7, Nakazawa discloses in figure 23b a second substrate (313) disposed opposing a surface of the first substrate. Nakazawa discloses in figure 23b liquid

crystals (312) sandwiched by the first substrate and the second substrate, and driven by transistor elements formed on the semiconductor layers.

With regard to claim 22, it should be noted that method of using limitations to not distinguish the prior art over the claimed invention. However, Nakazawa discloses in column 1, lines 6 – 8 an electronic equipment comprising the electro optical device.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazawa as applied to claim 1 above, and further in view of Watanabe et al. (USPAT 5316960, Watanabe).

Nakazawa does not disclose the semiconductor region forming the transistor comprises monocrystalline silicon. Watanabe teaches in column 4, lines 22 – 26 that monocrystalline silicon is a well known material with which to form a semiconductor region. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use monocrystalline silicon of Watanabe as the semiconductor for the transistor of Nakazawa in order to select a layer with desired channel characteristics.

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazawa as applied to claim 1 above, and further in view of one of ordinary skill in the art.

It has been held in In re Pearson 181 USPQ 641 (CCPA) that intended use does not avoid prior art. Therefore, it would have been obvious to use the device of claim 1 as an LCD projector.

11. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazawa as applied to claim 1 above, and further in view of Nishihara et al. (JPPAT 06163891, Nishihara).

Nakazawa does not teach that portions of the plurality of scanning lines form the gate electrodes. Nishihara teaches in figures 7 and 8 and in the portions of a scanning line (5) form gate electrode. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the portion of the scanning lines as part of the gate electrodes of Nishihara in the device of Nakazawa in order to decrease the cost of manufacturing the device by decreasing the number of masking steps needed.

Response to Arguments

12. Applicant's arguments filed September 26, 2002 have been fully considered but they are not persuasive.

13. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the lower end

in the gate length direction of the gate electrode extends outside of the gate line in the semiconductor region are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
October 22, 2002

GEORGE ECKERT
PRIMARY EXAMINER